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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/650,193	08/28/2003	Koichi Ohto	Q77191	6245

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EXAMINER

WILLIAMS, ALEXANDER O

ART UNIT	PAPER NUMBER
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2826

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PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.



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MAY -7 2008

In re Application of :
Koichi OHTO et al. :
Application No.: 10/650,193 :
Filed: August 28, 2003 :
For: SINGLE DAMASCENE STRUCTURE SEMICONDUCTOR :
DEVICE HAVING SILICON-DIFFUSED METAL WIRING :
LAYER :

NOTICE OF WITHDRAWAL
FROM ISSUE UNDER
37 CFR § 1.313

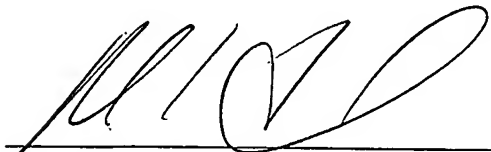
The purpose of this communication is to inform you that the above-identified application is being withdrawn from issue pursuant to 37 CFR 1.313.

The application is being withdrawn from issue because of unpatentability of at least one claim.

The issue fee is refundable upon written request. If however, the application is again found allowable, the issue fee can be applied toward payment of the issue fee in the amount identified on the new Notice of Allowance and Issue Fee Due upon written request. This request and any balance due must be received on or before the due date noted in the new Notice of Allowance in order to prevent abandonment of the application.

The above-identified application is being forwarded to the examiner for prompt appropriate action, including notifying applicant of the new status of this application.

Any question regarding this communication should be directed to Sue Purvis, Supervisory Patent Examiner, at (571) 272-1236.


Richard Seidel, Director
Technology Center 2800

Application/Control Number: 10/650,193
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Serial Number: 10/650193 Attorney's Docket #: Q77191
Filing Date: 8/28/03; claimed foreign priority to 5/8/02; 10/17/03; 5/5/03

Applicant: Ohto et al.

Examiner: Alexander Williams

This application is a continuation in part of application # 10/281321, filed 10/28/2002, now abandoned.

The indicated allowability of claims 3-7, 15-17, 51 and 215-218 are withdrawn in view of the newly discovered reference(s) to some of the references cited in the I.D.S. filed 3/14/07. Rejections based on the newly cited reference(s) follow.

Applicant's Amendment filed 5/12/06 to the election of Species I, figures 5A-8C (claims 1 to 17 and 51), filed 8/11/04, has been acknowledged.

Claims 1, 2, 8-14, 18-50 and 52-214 have been cancelled.

Claims 3-7, 15-17, 51 and 215-218 are rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claims 3, 15 and 215-218, it is unclear and confusing to what is meant by "a first **silicon**-diffused **metal** layer." Please explain how the silicon is diffused into the metal layer.

Any of claims 3-7, 15-17, 51 and 215-218 not specifically addressed above are rejected as being dependent on one or more of the claims which have been specifically objected to above.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 3-7, 15-17, 51 and 215-218, **insofar as they can be understood**, are rejected under 35 U.S.C. 102(e) as being anticipated by Noguchi Junji et al. (Japan Patent Application # 2003-347299).

Noguchi Junji et al. is referred to as cited Application 1.

Remarks

(1) Regarding the priority date of the present application and the filing date of the cited application.

This application claims domestic priority based on Japanese Patent Application 2002-132780 (hereinafter referred to as "first basic application") filed on May 8, 2002 (hereinafter referred to as "first priority date") and Japanese Patent Application 2002-302841 (hereinafter referred to as "second basic application") filed on October 17, 2002 (hereinafter referred to as "second priority date"). On the other hand, the filing date of Cited Application 1 is May 24, 2002, which is between the first priority date and second priority date. Thus, in the following, the inventions relating to Claims 3-7, 15-17, 51 and 215-218 of the present application and the descriptions of the Specification or Drawings initially filed in the first basic application and second basic application (hereinafter referred to as "Initial Specification, etc.") will be compared and the reference date (hereinafter referred to as "reference date") for determination of novelty and obviousness of the inventions relating to each of the claims will be considered, with the evaluation in comparison to Cited Application 1 being carried out only for inventions for which the reference date is after the second priority date.

(2) Content of the basic applications

The Initial Specification, etc. of the first basic application discloses an invention wherein silicide is formed on the surface of Cu wiring constituting single layer wiring. It is not found to make any disclosures regarding diffusing silicone so as not to form a silicide layer on the surface of Cu wiring or regarding a multilayer wiring structure. (Paragraph (0058) of the Detailed Description of the Invention of the first basic application states, "A

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mixed layer with Si contained in the Cu, without silicidization of the top surface of the Cu wiring 7, is also possible," but since the conditions for diffusing silicon in Cu such that silicidization does not take place are in no way disclosed in the first basic application, it cannot be said that the Initial Specification, etc. of the first basic application substantially discloses preventing a silicide layer from being contained on the Cu surface.)

Furthermore, the Initial Specification, etc. of the second basic application discloses an invention wherein silicon is diffused into Cu wiring constituting single layer wiring or multilayer wiring so as not to form a silicide, also providing disclosures regarding dual damascene technology and single damascene technology. Therefore, the inventions for which the reference date is the second priority date and does not go as far back as the first priority date can be said to include the portion of Claims 3-7, 15-17, 51 and 215-218 including stipulations regarding a multilayer wiring structure and the portion of Claims 3-7, 15-17, 51 and 215-218 where "the metal wiring does not contain a metal silicide layer."

(3) Claims for which the reference date is after the second priority date

Let us examine Claims 3-7, 15-17, 51 and 215-218 for the presence of stipulations regarding a multilayer wiring structure and as to whether they include a portion to the effect that "the metal wiring does not contain a metal silicide layer." The claims with stipulations regarding a multilayer wiring structure are Claims 3-5 and 7, and the claims which cite any one of those claims, i.e. Claims 6, 15-17, 51 and 215-218. Furthermore, all of Claims 3-7, 15-17, 51 and 215-218 include the case where "the metal wiring does not contain a metal silicide layer." Therefore, for Claims 2-5 and 7, and for the claims which cite any of those claims, i.e. Claims 6, 15-17, 51 and 215-218, the reference date is the second priority date. Furthermore, for the portion of Claims 3-7, 15-17, 51 and 215-218 where "the metal wiring does not contain a metal silicide layer," the reference date is the second priority date. (These inventions are to be evaluated in comparison with the inventions described in Cited Application 1.)

(4) Evaluation

The full text of the specification and the drawings initially appended to the application form of Noguchi Junji et al. (figures 1 to 36) Cited Application 1 describes diffusing silicon in copper wiring such that a silicide layer is not formed, and forming a wiring gap insulating film (corresponding to the "metal diffusion preventing film") over it. Therefore, Claims 3-5 and 7, and the claims which cite any of those claims, i.e. Claims 6, 15-17, 51 and 215-218, are identical or essentially identical to inventions described in Cited Application 1. Furthermore, the portion of the other claims where "the metal wiring does not contain a metal silicide layer" is identical or essentially identical to inventions described in Cited Application 1.

3. For example, in claim 3, Noguchi Junji et al. (figures 1 to 36) specifically figure 13 show a semiconductor device 1 comprising: an insulating underlayer 15; a first insulating interlayer **NWL,PWL** formed on said insulating underlayer, said first insulating

interlayer having a groove (**in which 6,7 sits within NWL,PWL**); a first silicon-diffused metal layer **6,7** therein buried in said groove; and a first metal diffusion barrier layer (**6,7**) formed on said first silicon-diffused metal layer (**layer above 6,7**) and said first insulating interlayer, wherein said first insulating interlayer comprises at least one of a SiO₂ layer, a SiCN layer, a SiC layer, a SiOC layer and a low-k material layer and said low-k material layer comprises one of a ladder-type hydrogen siloxane layer and a porous ladder-type hydrogen siloxane layer.

15. For example, in claim 15, Noguchi Junji et al. (figures 1 to 36) specifically figure 13 show a semiconductor device **1** comprising: an insulating underlayer **15**; a first insulating interlayer **NWL,PWL** formed on said insulating underlayer, said first insulating interlayer having a groove (**in which 6,7 sits within NWL,PWL**); a first silicon-diffused metal layer **6,7** therein buried in said groove; and a first metal diffusion barrier layer (**layer above 6,7**) formed on said first silicon-diffused metal layer and said first insulating interlayer; and a first etching stopper **2** between said insulating underlayer and said first insulating interlayer.

216. Noguchi Junji et al. (figures 1 to 36) specifically figure 13 show a semiconductor device **1** comprising: an insulating underlayer **15**; a first insulating interlayer **NWL,PWL** formed on said insulating underlayer, said first insulating interlayer having a groove (**in which 6,7 sits within NWL,PWL**); a first silicon-diffused metal layer **6,7** including no carbon therein buried in said groove; an a first metal diffusion barrier layer (**layer above 6,7**) formed on said first silicon-diffused metal layer and said first insulating interlayer, wherein said first metal diffusion barrier layer comprises at least one of a SiCN layer, a SiC layer, a SiOC layer and an organic material layer.

217. Noguchi Junji et al. (figures 1 to 36) specifically figure 13 show a semiconductor device **1** comprising: an insulating underlayer **15**; a first insulating interlayer **NWL,PWL** formed on said insulating underlayer, said first insulating interlayer having a groove (**in which 6,7 sits within NWL,PWL**); a first silicon-diffused metal layer **6,7** including no carbon therein buried in said groove; and a first metal diffusion barrier layer (**layer above 6,7**) formed on said first silicon-diffused metal layer and said insulating interlayer, further comprising a first etching stopper between said insulating underlayer and said first insulating interlayer.

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218. Noguchi Junji et al. (figures 1 to 36) specifically figure show a semiconductor device **1** comprising: an insulating underlayer **15**; a first insulating interlayer **NWL,PWL** formed on said insulating underlayer, said first insulating interlayer having a groove (**in which 6,7 sits within NWL,PWL**); a first silicon-diffused metal layer **6,7** including no carbon therein buried in said groove, and a first metal diffusion barrier layer (**layer above 6,7**) formed on said first silicon-diffused metal layer and said first insulating interlayer, wherein said first etching stopper comprises at least one of s SICN layer, a SiC layer, a SiOC layer and an organic material layer.

Applicant cannot rely upon the foreign priority papers to overcome this rejection because a translation of said papers has not been made of record in accordance with 37 CFR 1.55. See MPEP § 201.15.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.

Patentability shall not be negated by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(f) or (g) prior art under 35 U.S.C. 103(a).

Claims 3-7, 15-17, 51 and 215-218, **insofar as they can be understood**, are rejected under 35 U.S.C. 103(a) as being unpatentable over Noguchi Junji et al. (Japan

Patent Application # 2003-347299) in view of Noguchi Junji et al. (Japan Patent Application # 2001-291720).

Noguchi Junji et al. '299 is referred to as Cited Literature 1.

Noguchi Junji et al. '720 is referred to as Cited Literature 2.

(I) Cited Literature 2

Remarks See the full text of Cited Literature 2 (especially Figure 56 and related passages).

According to Figure 56, the copper wiring formed by the manufacturing method of Cited Literature 1 (NH₃ plasma treatment) contains silicon which does not form silicide. Therefore, the copper wiring described in Cited Literature 2 and the metal wiring with diffused silicon of the present invention cannot be distinguished, and thus, it must be concluded that the inventions relating to Claims 3-7, 15-17, 51 and 215-218 of the present application are identical to inventions described in Cited Literature 2, or could be easily invented by a person skilled in the art based on inventions described in Cited Literature 2.

Applicant cannot rely upon the foreign priority papers to overcome this rejection because a translation of said papers has not been made of record in accordance with 37 CFR 1.55. See MPEP § 201.15.

Claims 3-7, 15-17, 51 and 215-218, **insofar as they can be understood**, are rejected under 35 U.S.C. 103(a) as being unpatentable over Imai Toshinoro et al. (Japan Patent Application # 2000-150517) in view of Sekiguchi Mitsuru (Japan Patent Application # 2000-058544).

Imai Toshinoro et al. is referred to as Cited Literature 3.

Sekiguchi Mitsuru is referred to as Cited Literature 4.

Cited Literature 3 and 4 Remarks See the full text of Cited Literature 3. Also see the full text of Cited Literature 4. In the inventions described in Cited Literature 3 and 4, a silicide layer is formed over a copper wiring surface, and it is found that silicon diffuses into the copper wiring during forming of the silicide layer, so it must be concluded that

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the inventions relating to Claims 1-10, 12-18, 20, 21, 23-80, 82-84, and 86-109 are identical to inventions described in Cited Literature 3 and 4 or could be easily invented by a person skilled in the art based on inventions described in Cited Literature 3 and 4.

Field of Search	Date
U.S. Class and subclass: 257/750,750,758,257,774,762,759,774,751,635,636,640,7 52,e23.144,e23.167,e23.145	11/1/04 5/14/05 1/23/06 7/22/06 4/14/08
Other Documentation: foreign patents and literature in 257/750,750,758,257,774,762,759,774,751,635,636,640,7 52,e23.144,e23.167,e23.145	11/1/04 5/14/05 1/23/06 7/22/06 4/14/08
Electronic data base(s): U.S. Patents EAST	11/1/04 1/23/06 7/22/06 4/14/08

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alexander O. Williams whose telephone number is (571) 272 1924. The examiner can normally be reached on M-F 6:30AM-7:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sue Purvis can be reached on (571) 272 1236. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Alexander O Williams/
Primary Examiner, Art Unit 2826

/AOW/
4/14/08